IN THE SPECIFICATION:

Please replace paragraph [0022] at page 5 as follows:

**[0022]** Similarly, the falling edge of CLK causes flip-flop 106 to latch the logic state of the data input signal DATA. When latched, output signal ~~108~~ 110 carries DATA (D1 and D3). Since CLKZ is now high, AND gate 114 passes output signal ~~108~~ 110 to OR gate 116, which produces that DATA (D1 and D3) at Qout. At the same time, since CLK is low, AND gate 112 does not pass any data to OR gate 116. As such, DATA is passed to Qout whenever there is a rising or a falling edge.

Please replace paragraph [0031] at page 8 as follows:

**[0031]** Between t2 and t3, CLK is set to a logical zero and CLKZ to a logical one. During this period, both SW1 and SW2 are turned off, while both SW0 and SW3 are turned on. As a result, data signal 304 carries new DATA (D1 and D2), while output signal 314 carries the inverted DATA (D1Z and D2Z). The output signal 316 passes the DATA (D1Z) that is stored at the NAND gate ~~308~~ 310 through SW3 to input signal 318. Through the inverter 320, Qout now carries DATA (D1).